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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/092,158	06/05/1998	SAILESH M. MERCHANT	MERCHANT3333	5736

47396 7590 02/17/2005

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/092,158	MERCHANT ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-12, 16, 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 5,591,671) in view of Bai et al. (U.S. 5,714,418) and Teo (U.S. 5,970,374).

In reference to claims 1, 7, 12, 18 and 24, Kim et al. (Figs.2-4) in a related method to form an interconnect layer teach the steps of forming a contact opening (25) in a dielectric layer (24) on a semiconductor substrate (21, 24), said contact opening (25) electrically contacting an active device; depositing by physical vapor deposition (PVD) a barrier layer (26, 27) in said contact opening (25) and on at least a portion of said semiconductor substrate (21, 24), said barrier layer deposition step includes depositing titanium layer (26) and depositing titanium nitride layer (27) on said titanium layer (26); depositing a contact metal (28) on said barrier layer (26, 27) within said contact opening (25); removing a substantial portion of said contact metal (28) and said barrier layer (26, 27) from said semiconductor substrate (21, 24) to form a contact plug within said contact opening (25) (column 5, lines 24 – 39); and subjecting said contact plug to a heating treatment, changing the crystalline structure (i.e., annealing) of the barrier layer (26, 27) to reduce ohmic contact (column 4, line 27 – column 6, line 56).

Kim et al. fail to teach extending the plug to an uppermost surface of said substrate. However, Bai et al. (Figs.4C-4D) in a related method to form planarized interconnects in a semiconductor device teach the steps of removing a substantial portion a contact metal (44) and a barrier layer (42, 43) from a semiconductor substrate (40, 41) to form a contact plug within a contact opening (47), said plug extending to an uppermost surface of said substrate (40, 41) (column 9, lines 12-25). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Kim et al. and Bai et al. to enable the removing step of Kim et al. to be performed according to the teachings of Bai et al. because this would isolate the interconnect layer within the trench (column 9, lines 18 – 20) and because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed removing step of Kim et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Kim et al. and Bai et al. fail to teach wherein said heat treatment is a rapid thermal anneal process performed from about 5 to 60 seconds, at a temperature from about 600°C to about 750°C. However, Teo in a related method to form interconnects teaches the step of using rapid thermal annealing to a Ti/TiN layer at a temperature of about 670°C for about 30 seconds (column 3, lines 30 – 35 and column 4, lines 17-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a RTA process as taught by Teo

and in the combination of Kim et al. and Bai et al., since this improves the adhesion of the barrier layer in the contact opening (column 4, lines 17-25).

Still the combined teachings of Kim et al., Bai et al. and Teo fail to teach performing the thermal anneal from 5 to 60 seconds at a temperature form about 600°C to 750°C. However, in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. MPEP 2144.05. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the annealing specifications disclosed in the combined teachings of Kim et al., Bai et al. and Teo to arrive at the claimed invention.

In reference to claims 5, 6, 16 and 17, the combined teachings of Kim et al., Bai et al. and Teo teach depositing a tungsten contact by chemical vapor deposition (Kim et al., column 4, line 57 – column 5, line 4).

In reference to claims 8, 9, 19, 20 and 23, Kim et al. in combination with Bai et al. and Teo teach depositing a barrier layer including forming a thickness of said barrier layer ranging from about 90 nm to about 290 nm within said contact opening having a design width below 1μ and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater (Kim et al., column 4, lines 38-44). Kim et al. in combination with Bai et al. fail to teach the thickness of said barrier layer from about 5 nm to about 20 nm and having 5% to about 20% of field area thickness within said contact opening. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions

because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In reference to claims 10, 11, 21 and 22, Kim et al. in combination with Bai et al. and Teo teach removing a substantial portion including removing said contact metal and said barrier layer from said field area thickness by chemical mechanical polishing processes (Kim et al., column 5, lines 62-67 and Bai et al., lines column 9, lines 12-24).

3. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. ('671) in view of Bai et al. ('418) and Teo ('374) as applied to claims 1, 5-12, 16, 17-24 above, and further in view of the applicants admitted prior art in the instant application.

Kim et al. in combination with Bai et al. and Teo teach depositing a barrier layer in a contact opening in a dielectric layer, but fail to show the contact opening with an aspect ratio ranging from about 3:1 to about 5:1. However, the prior art teaches forming openings having aspect ratios from about 3:1 to about 5:1 (page 2, lines 1-6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify aspect ratios of about 3:1 to about 5:1 as taught by the prior art and include it in the combination of Kim et al. and Bai et al., since this fulfill the need for forming smaller devices (page 1, line14 - page 2, line 6).

Response to Arguments

4. Applicant's arguments filed 11/22/2004 have been fully considered but they are not persuasive.

In reference to Kim et al., applicants argue, "...there is no teaching or suggestion that the metal pattern formed in this embodiment is a contact plug with an uppermost surface extending to the surface of the ~~surface~~ substrate. The applicants submit that forming a metal pattern likely refers to the process of transferring the layout of a circuit design on to a substrate...". In response to this argument, Kim et al. was relied on forming a patterned plug (column 5, lines 24 – 39) which is open not only to "the process of transferring the layout of a circuit design on to a substrate" as argued by the applicants, but also to form metal plugs.

Also, applicants argue, "...Regarding the disclosure that Teo's heating process improves the adhesion of the barrier layer, the Applicants wish to point out that Teo teaching performing the RTA on the metal-free contact opening as shown in Fig.3A. There is no teaching or suggestion by Teo of subjecting a contact plug to a temperature from about 600°C to about 750°C, as recited in Claim 1...". In response to this argument, Teo was relied on the teaching of performing an RTA process on a Ti/TiN layer at a temperature of 670°C for about 30 seconds improves the adhesion of the

barrier layer in the contact opening. Teo was not relied on whether the RTA is performed at certain point during the manufacture of the semiconductor device.

Furthermore, Applicants argue, "...The Applicants maintain that there is no reason why one skilled in the art would be motivated to heat Kim ohmic contact and barrier layers beyond Kim's limit of 550°C, based on Teo's teachings...". In response to this argument, and as mentioned above, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a RTA process as taught by Teo and in the combination of Kim et al. and Bai et al., since this improves the adhesion of the barrier layer in the contact opening (column 4, lines 17-25).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
February 8, 2005

George Fourson
Primary Examiner